

7-18-03

<b>FORM PTO-1449 (SUBSTITUTE)</b>  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  <b>INFORMATION DISCLOSURE          STATEMENT BY APPLICANT</b> (37 CFR 1.98(b))				Attorney Docket No.: M&N-IT-466 Appl. No.: <u>10 623067</u>  Applicant: ERIC LIAU  Filing Date: July 18, 2003 Group Art Unit: <u>2825</u>			
EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
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<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)</b>							
BT		Hsiao, M. S. et al.: "Sequential Circuit Test Generation Using Dynamic State Traversal", European Design and Test Conference, March 1997, pp. 22-28					
BT		Singer, S. et al.: "Virtual Test Automation Generator (VTAG)", Navair Lakehurst, May 5, 2000, pp. 1-10					
EXAMINER <u>BT</u>				DATE CONSIDERED <u>08/05/05</u>			
EXAMINER Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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<u>BT</u>		Rudnick, E. M. et al.: "Automatic Test Generation", "Genetic Algorithms for VLSI Design, Layout and Test Automation", Prentice Hall, Upper Saddle River, NY, 1999, pp. 159-166 and pp. 179-184					
EXAMINER <u>[Signature]</u>				DATE CONSIDERED <u>9/20/04</u>			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							